

Dislocation Density and Sheet Resistance Variations Across Semi-Insulating GaAs Wafers

ROY T. BLUNT, STEPHEN CLARK, AND DEREK J. STIRLAND

Abstract—Dislocation densities and sheet resistances have been measured across (001) orientated wafers cut from Cr-doped liquid encapsulated Czochralski (LEC) grown semi-insulating (SI) GaAs boules. A defect-sensitive etch was used to reveal dislocations while a novel scanning technique has been developed for measurement of sheet resistance. The general patterns of dislocation density and sheet resistance variations are shown to be similar at the seed end of the crystal. Both agree well with recent work on electron trap density variations across a GaAs wafer and with a theoretical study of the genesis of dislocations during LEC growth of GaAs. Dislocation interactions during crystal growth have been shown to occur even at the seed end of the boule. The pattern of sheet resistance variations across wafers is shown to change down the length of the boule.

I. INTRODUCTION

SEMI-INSULATING GaAs is used as a substrate for both epitaxial growth of doped layers and for direct ion implantation in the manufacture of GaAs IC's. The GaAs boules are grown by either liquid encapsulated Czochralski (LEC) or Bridgman techniques, and it is generally recognized that there are significant resistivity and dislocation density variations along the length of the boule. However, little attention appears to have been paid to the possibility of parameter variations across wafers cut from these boules. It is clear that attempts to obtain uniformity over large areas by, for example, ion implantation may be invalidated if critical substrate parameters vary across the wafer and these variations are then reflected in device parameters. As part of our GaAs IC program we have looked at variations in both dislocation density and electrical uniformity across wafers cut from LEC pulled semi-insulating boules.

It is obvious that severe variations in sheet resistance across a semi-insulating wafer can affect device isolation on an IC. The effects of dislocation density variations on majority carrier devices is still uncertain although current thinking [1] is that dislocation densities of $\sim 3 \times 10^4 \text{ cm}^{-2}$ in undoped semi-insulating substrates do not affect device performance.

We have measured dislocation densities by conventional etching techniques and electrical uniformity by a novel

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technique which we term the 'dark spot' method. Both parameters will be shown to follow a similar pattern to the Jordan [2], [3] theoretical model of dislocation densities in LEC pulled GaAs crystals near the seed end of the boule. However, the pattern changes towards the tail end of the boule.

II. DISLOCATION DENSITY DETERMINATIONS

Unless otherwise stated, all of the work to be reported here was carried out on polished wafers of Cr-doped semi-insulating GaAs cut from near the seed end of a single (001) axis unground LEC grown boule approximately 57 mm in diameter with a natural (110) growth flat.

Dislocation densities were obtained using the A/B etch devised originally by Abrahams and Buiocchi [4] because it has a higher effective resolution than 'orthodox' etches [5]. To avoid errors due to mechanical damage introduced during specimen preparation, some 30 μm of material was removed from the surface using a polish etch solution of $3\text{H}_2\text{SO}_4 : 1\text{H}_2\text{O}_2 : 1\text{H}_2\text{O}$ [6] prior to the application of the A/B etch for 5 min at room temperature, which removed a further 12 μm of material.

Fig. 1 shows the location of photomicrographs taken on a (110) axis bounded quadrant of the substrate wafer. Altogether, some 140 micrographs were taken at a magnification of $65\times$ using Nomarski interference contrast techniques. One side of each micrograph was set parallel to a defined (110) direction on the wafer. Micrographs with overlapping areas were obtained from the center to the slice peripheries along the [110], [010], and [1̄10] directions. Additional sets were taken along directions at 14° and 26.5° to the [110] and [1̄10] directions. The position of individual micrographs was defined using the X, Y coordinate measurements on the microscope specimen stage. An extra set of measurements was also made along the [110] radius of the wafer.

Fig. 2 shows three micrographs from the set which lie along the [1̄10] direction from substrate center to substrate edge. These photomicrographs show typical A/B etched surfaces as seen under the optical microscope using Nomarski interference contrast. The black/white contrast lines are ridges which indicate dislocations previously existing in the material removed by the A/B etch. From such

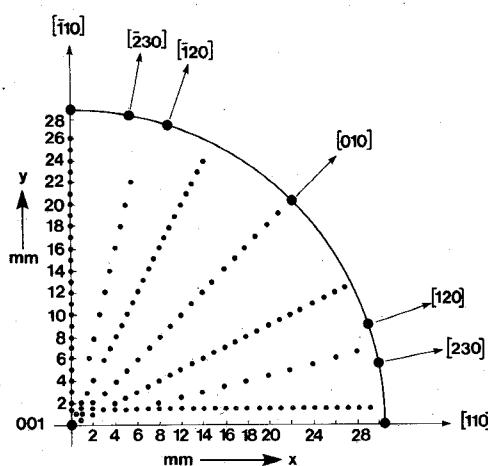


Fig. 1. Location of micrographs in substrate quadrant.

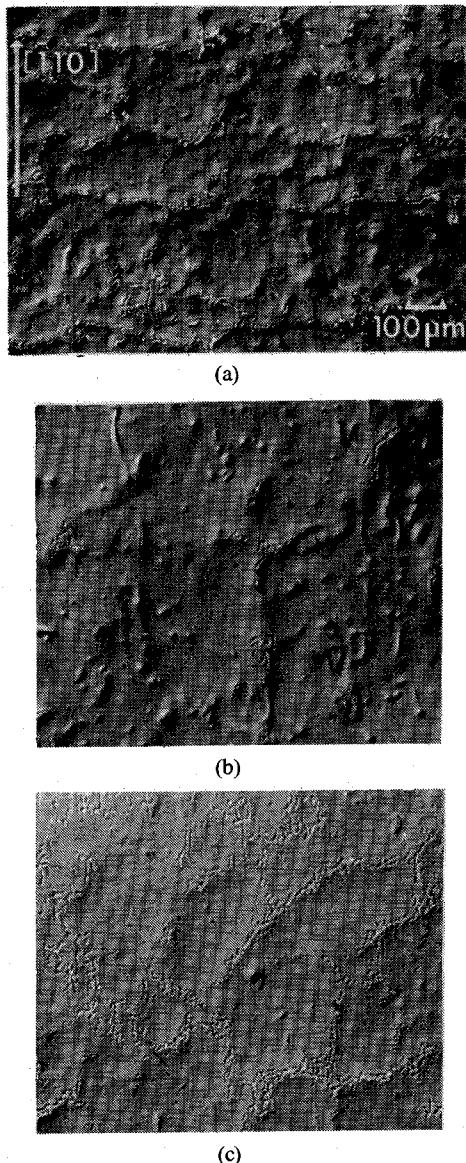
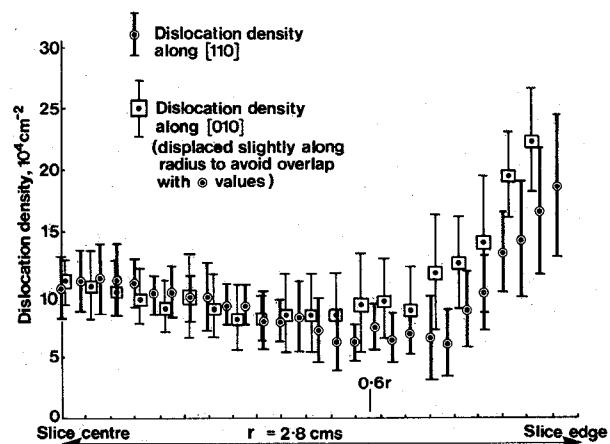
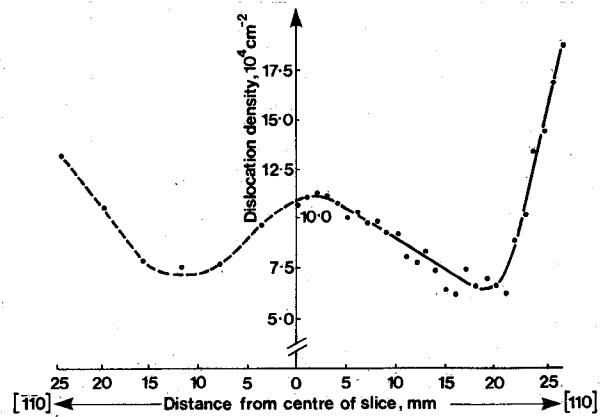
Fig. 2. Photographs of etched surfaces (after Clark and Stirland [7]). (a) At center (0,0). (b) At $0.6r$ (0,17). (c) Near $[110]$ edge (0,25).Fig. 3. Experimentally determined dislocation densities along [110] and $[010]$ radii.

Fig. 4. Experimentally determined dislocation densities along [110] diameter.

photomicrographs actual values of dislocation densities were obtained using the so-called intercept method [7], [8]. These dislocation density values represent the dislocation density in $\{110\}$ planes normal to the (001) surface. Fig. 2(a) is from an area close to the center of the wafer and gives a value of 1.1×10^5 dislocations cm^{-2} . Fig. 2(b) shows the minimum dislocation density of $5.8 \times 10^4 \text{ cm}^{-2}$ seen along this axis, taken at ~ 0.6 of the radius distance from the center of the wafer. Fig. 2(c) shows an area close to a $[110]$ edge of the wafer, with a total dislocation density of $1.3 \times 10^5 \text{ cm}^{-2}$.

Fig. 3 shows experimentally determined dislocation density variations along the $[110]$ axis and along the $[010]$ axis at 45° to it. The bars represent standard deviations for each set of measurements, and indicate the variability of dislocation distribution across the area of the micrographs rather than the experimental errors in the density values. The most significant features to note are the high values at the perimeter of the wafers, the pronounced minimum at ~ 0.6 radius on the $[110]$ axis, and the slightly less pronounced minima along the $[010]$ axis. Fig. 4 shows a plot of the dislocation density across a complete $\langle 110 \rangle$ diameter of

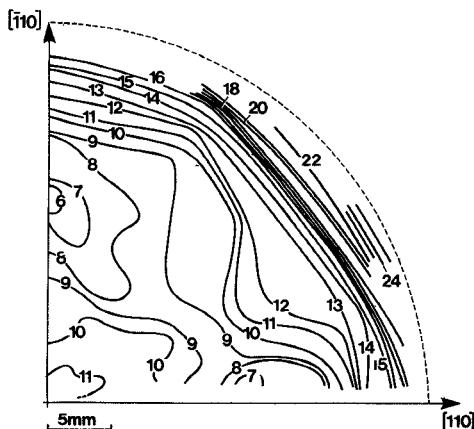


Fig. 5. Experimentally determined dislocation density contour lines. Units of $1 \times 10^4 \text{ cm}^{-2}$.

the slice. The full line shows results obtained along the [110] radius of the quadrant from 27 experimental determinations, while only six measurements were made across the [110] radius (dashed line). It should be noted that the main features of the plot (i.e., maximum at the outside edges, minimum at ~ 0.6 radius, and secondary maxima at the center of wafer) are reproduced in both radii but that there is a slight asymmetry between absolute values on the two radii.

Fig. 5 shows the experimentally determined dislocation density contours over the complete quadrant. The contour lines represent mean dislocation density increments of $1 \times 10^4 \text{ cm}^{-2}$. Note the absolute maxima along the [010] edge with the lower maxima at $\langle 110 \rangle$ edges and at the center. Pronounced minima can be seen along the [110] and [110] axes at ~ 0.6 radius. Recent papers by Jordan and co-workers [2], [3] have described a theoretical model for the thermo-elastic analysis of dislocation generation in LEC grown GaAs crystals. This work extends the earlier theories of Billig [9], Penning [10], and Brice [11] which postulate that the primary cause of the observed dislocation patterns is the partial relief of the severe thermal stresses which arise during the crystal growth process. As the crystal cools down, the outside surface of the boule is held in tension while the core is in compression resulting in the formation of a relatively unstrained annular region. The model first computes the temperature distribution in the growing crystal as a function of pull rate and ambient temperature and then calculates the radial, tangential, and axial stress components induced by this temperature distribution. From these stresses it was possible to calculate the resolved shear stress components along the twelve $\{111\} \langle 110 \rangle$ slip systems and, where these exceeded critical values, it was postulated that the excess stress was proportional to the number of generated dislocations.

Fig. 6 shows the computed dislocation densities for the seed end of a $\langle 001 \rangle$ axis GaAs LEC boule, reproduced (partially) from Jordan *et al.* [3]. The contour lines represent values of the so-called resolved shear-stress compo-

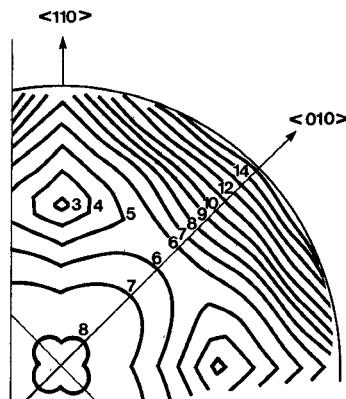


Fig. 6. Theoretical dislocation density contour lines for the top wafer of an $\langle 001 \rangle$ GaAs boule. Reproduced partially from Jordan *et al.* [3, Fig. 6]. (Copyright 1980 American Telephone and Telegraph Company—reprinted by permission.)

nents which should be proportional to the number of slip-induced dislocation densities. Note the very pronounced similarities between this theoretically calculated plot and our experimental data. In particular, highest dislocation densities are predicted at the $\langle 010 \rangle$ edges, with secondary maxima both at the $\langle 110 \rangle$ edges and the center. Note also the pronounced minima along the $\langle 110 \rangle$ axes at about the 0.6 radius points.

However, the experimentally determined contour map does not have the perfect four-fold symmetry predicted by theory. One possible reason for this could be the use of closely spaced contours (1×10^4 per line) on the experimental plot when the experimental spread of values about 1×10^5 dislocations cm^{-2} is $\pm 2-3 \times 10^4$. However, if the contours are replotted at larger intervals the overall configuration of the dislocation distribution does not alter. The departure from strict four-fold symmetry is thus considered to be genuine. The GaAs crystal structure (sphalerite) belongs to the space group $F\bar{4}3m$ which exhibits two-fold symmetry and therefore the dislocation pattern itself might be expected to show a two-fold symmetry. Abrahams *et al.* [12] have demonstrated experimentally, and from symmetry considerations, that an asymmetry exists even relative to orthogonal 60° dislocations of the same sign in the sphalerite structure.

Possible reasons for discrepancies between experiment and theory are, firstly, that a loss of crystal symmetry may occur due to growth conditions and, secondly, that dislocation interactions may occur during growth. The first is unlikely since any asymmetry capable of causing this effect would have to rotate with the crystal. The second suggestion is probable since Jordan has emphasized that his model is essentially descriptive of the *generation* of thermal stress induced dislocations only and that the distributions will be modified when dislocation interactions are considered.

The effects of dislocation interactions by both climb and glide processes are shown in Fig. 7, which shows an area close to an $\langle 010 \rangle$ edge. Here dislocations have clustered

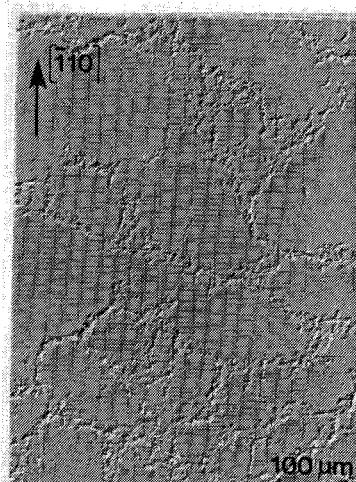


Fig. 7. Cellular structure near [010] edge of slice.

into walls to form a pronounced cellular structure with essentially dislocation-free areas within the cells. A similar, though less pronounced effect, can be seen in Fig. 2(c). A different form of dislocation bunching can be seen in central areas of the boule (Fig. 2(a)) where the dislocation lines collect along the orthogonal $\langle 110 \rangle$ directions. However, despite the clear evidence for considerable dislocation interactions and rearrangements subsequent to formation, it is evident that the overall variations are still similar to those predicted theoretically.

III. SHEET RESISTANCE MEASUREMENTS

Although work has been carried out on resistance variations across Czochralski pulled silicon boules [13], little work has been published on the variations of sheet resistance across semi-insulating GaAs boules. This has probably been due to the difficulty in making accurate and reproducible sheet resistance measurements on semiconductor materials with sheet resistances in the $10^7 \rightarrow 10^{10} \Omega/\text{square}$ range. The elegant and nondestructive sheet resistance mapping technique developed by Blackburn [13] is unsuitable for very high resistance materials, while two- and four-probe methods used on GaAs give irreproducible results due to nonohmic contacts and space charge injection. The van der Pauw technique [14], [15] probably provides the best approach but, unless great care is taken, results can still be erratic. This method is also destructive and any form of large-scale area mapping would be very tedious. To overcome most of these problems we have developed a novel technique for electrical uniformity mapping which we term the 'dark spot' method. It is essentially nondestructive, simple, quick, reproducible, and readily amenable to automation.

First, consider a strip of semi-insulating GaAs with silver paste electrodes at each end. In the dark, the GaAs will have a very high resistance ($\sim 10^8 \Omega/\text{square}$) and the contacts will be nonohmic. If the GaAs is now strongly illuminated with white light, a large number of electron-hole pairs will be generated close to the surface, and the sheet resistance will fall to $\sim 10^6 \Omega/\text{square}$. The large number of

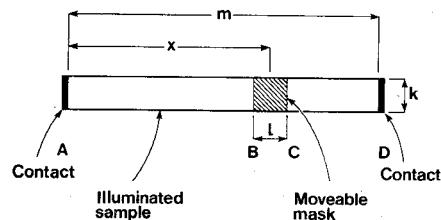


Fig. 8. Dark spot specimen layout (schematic).

carriers present close to the electrodes will ensure these are essentially ohmic in nature. Current-voltage plots show this to be true over the conditions used.

Now consider the situation shown in Fig. 8, of a uniformly illuminated strip of SI GaAs, of width k and length m , between contacts at ends A and D , with a movable mask preventing the light reaching a small portion BC of length l . For simplicity, let $k = l$. The situation now is that we have a total length $m - l$ of illuminated material of resistivity ρ_L and a length l of nonilluminated material of sheet resistance ρ_D . The contacts A and D are illuminated and thus provide low resistance contacts which can be neglected in a simple analysis. The total resistance R between the contacts is given by the expression

$$R = \frac{m - l}{k} \rho_L + \frac{l}{k} \rho_D. \quad (1)$$

If we take convenient values for k , l , and m of 5 mm, 5 mm, and 50 mm, respectively, then, provided the level of illumination is high enough to make the ratio ρ_D/ρ_L greater than 10, the value of $(l/k)\rho_D$ is comparable to or greater than $((m - l)/k)\rho_L$. The values of k , l , m , and R are easily determined experimentally.

If the dark area is now scanned from A to D by varying x , then, provided the contacts remain illuminated, the value of $((m - l)/k)\rho_L$ is constant and thus the variation of ρ_D with x can be determined by monitoring the total resistance R . Since ρ_L is much less than ρ_D , and is effectively averaged across the strip, variations in ρ_L caused, for instance, by small nonuniformities in illumination intensity, do not affect the measurement of ρ_D significantly. Any contact resistance effects at the electrodes are constant and do not affect the measurement, provided the edges of the contacts are illuminated.

Although the example of a simple strip of material is used above for simplicity, the method can be extended to cover complete wafers, as shown in Fig. 9, by using a fixed mask to prevent light reaching the material on either side of the uniform width strip to be measured. The concept can also be extended to cover sheet resistance mapping over the complete area of a circular wafer by sequentially illuminating and scanning strips between opposite pairs of electrodes as shown in Fig. 10.

Fig. 11 shows the results obtained on scanning across the $\langle 110 \rangle$ diameter of a Cr-doped SI LEC GaAs wafer adjacent in the boule to the one used for dislocation density measurements. All of the dark spot results to be presented here were obtained using a dark spot size of $5 \text{ mm} \times 5 \text{ mm}$. It should be noted that this method actually measured the

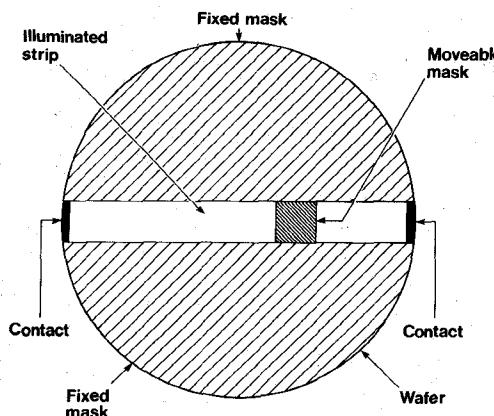


Fig. 9. Extension of method to full wafers (schematic).

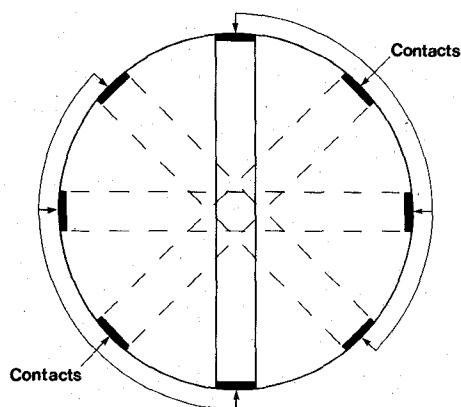


Fig. 10. Mapping over full area of wafer (schematic).

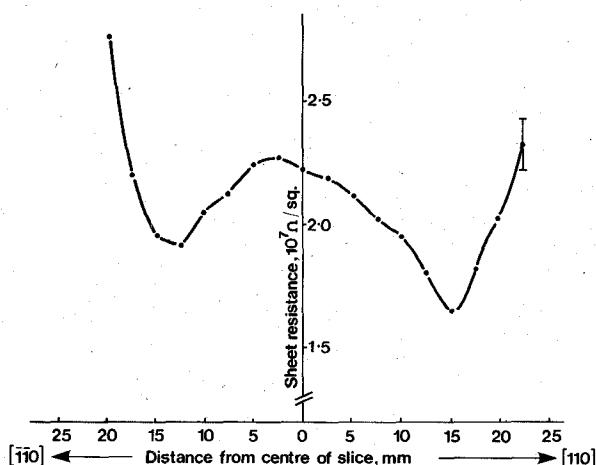


Fig. 11. Dark spot sheet resistance plot across [110] diameter.

resistance of the dark spot area of the GaAs—this is not the same value as the sheet resistance measured by the van der Pauw method. The dark spot resistance is lower than the van der Pauw value but appears to be proportional to it. The absolute value of the dark spot resistance is also affected by variations in both dark spot geometry and light intensity—however, the relative values across the slice remain identical. Thus, the method cannot, at present, be considered as giving absolute values of sheet resistance. It does, however, provide an excellent method for determining uniformity of sheet resistance across a slice. The shape

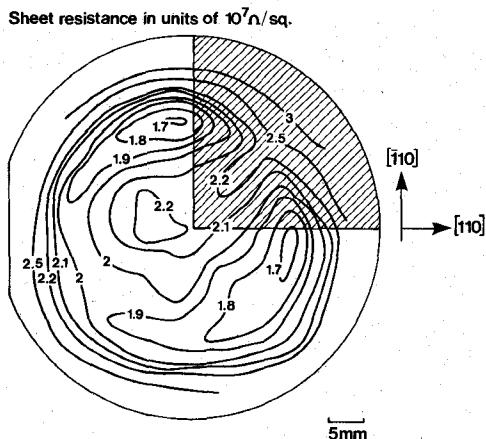


Fig. 12. Dark spot sheet resistance contour map of wafer.

of the plot across the wafer is highly reproducible from both run-to-run on a given wafer, and also from one wafer to another adjacent wafer from the same boule. 'Front' and 'back' surface measurements on double polished specimens show essentially identical results. The steep rise in resistance seen at the outer edges of the slice is genuine, and is not an edge effect caused by the measurement technique.

If Figs. 4 and 11 are compared, it can be seen just how similar the dark spot resistance plots are to the dislocation density plots. The great majority of both dark spot resistance and dislocation density plots across $\langle 110 \rangle$ diameters of (001) semi-insulating LEC GaAs wafers from the seed ends of the boule have shown very similar shaped plots, although in most cases there is far less imbalance between the two radii than shown in Fig. 11. There is little difference between plots obtained for Cr-doped and undoped boules. It is interesting to note that Martin *et al.* [16] have published a plot of EL2 trap densities across the $\langle 110 \rangle$ diameter of a Cr-doped LEC GaAs wafer which again shows the characteristic 'W' shaped plot seen in this work. Recent work [17], [18] on Cr concentrations across Cr-doped GaAs boules have, in contrast, shown no similar Cr concentration across the wafers.

Fig. 12 shows a contour plot obtained by the dark spot method. The plot shows that the resistance values are at their highest near the outside edges of the wafer and exhibit minima at about the half radius points—rising again towards the center of the slice. Stronger minima are seen along $\langle 110 \rangle$ directions and it appears that the geometric center of the wafer is not quite coincident with central sheet resistance maxima. The shaded area corresponds to the area used for the dislocation density plots shown in Fig. 5 and exhibits the same main features.

Most SI GaAs wafers taken from the seed end of boules have shown similar shaped patterns across the $\langle 110 \rangle$ axes to those predicted by Jordan's theory for the variations of dislocation densities in LEC pulled GaAs. However, as explained earlier, this model is only applicable to the generation of dislocations and will not apply strictly when interactions occur between dislocations. We have made a series of dark spot resistance plots across the $\langle 110 \rangle$ axes of five wafers cut from different positions between seed and

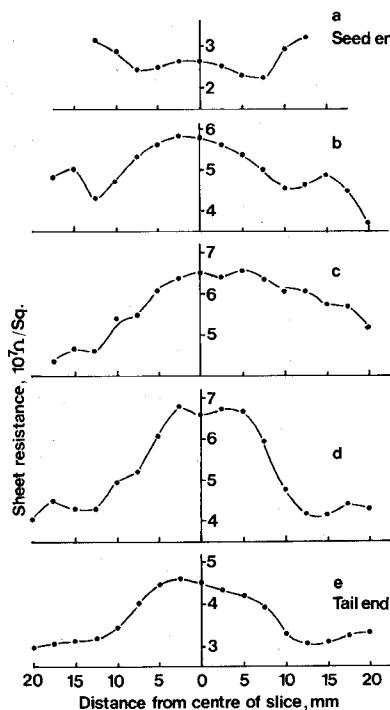


Fig. 13. Dark spot sheet resistance measurements along $\langle 110 \rangle$ diameters of wafers taken from various positions along a boule.

tail ends of a second Cr-doped LEC boule (i.e., a different boule from that used to obtain results shown in Figs. 1-12). The results are shown in Fig. 13. Note that the seed-end plot shows the usual 'W' shaped pattern as predicted by Jordan's theory. This becomes less pronounced as we go towards the tail end of the boule, finally tending towards a single central peak at the tail end itself. Similar results have been obtained on repeating the dark spot measurements down the length of a further boule and results taken from the tail-end slices of other boules have generally shown a central peak rather than the typical 'W' shaped pattern seen at the seed end. Very limited work on the dislocation density across a $\langle 110 \rangle$ axis of a single tail-end slice has shown a roughly 'M' shaped distribution, i.e., essentially the inverse of the distribution seen at the seed end.

IV. CONCLUSIONS

Dislocation densities and sheet resistances have been measured across (001) wafers cut from LEC pulled semi-insulating GaAs boules. Both parameters show very similar spatial variations across the wafer at the seed end of the boule. The patterns are very similar to those predicted by Jordan's theoretical model for the generation of dislocations in GaAs, despite the fact that some dislocation interactions have been shown to occur. The patterns are also similar to those exhibited for the variation of the EL2 trap density across wafers by Martin. Sheet resistance measurements on wafers cut at positions down the axis of the boule show that these patterns are only followed closely at the seed end of the boule. Considerable variations in the patterns occur towards the tail end of the boules.

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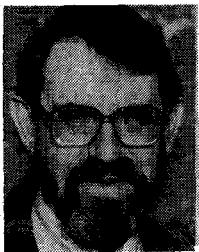
of producing GaAs IC's.

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Stephen Clark was born in Northampton, England, on June 12, 1962. He completed his secondary education at Campion School near Northampton by gaining a place at Queens' College, Cambridge. Before embarking on his higher academic studies, he spent 1980-1981 at the Allen Clark Research Centre as a Pre-University student, and is now in his first year at Queens' College reading Natural Sciences.



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He is a member and past secretary of the British Association for Crystal Growth.

Compensation Mechanism in Liquid Encapsulated Czochralski GaAs: Importance of Melt Stoichiometry

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Abstract—It is shown that the key to reproducible growth of undoped semi-insulating GaAs by the liquid encapsulated Czochralski (LEC) technique is the control over the melt stoichiometry. Twelve crystals were grown from stoichiometric and nonstoichiometric melts. The material was characterized by secondary ion mass spectrometry, localized vibrational mode far infrared spectroscopy, Hall-effect measurements, optical absorption, and photoluminescence. A quantitative model for the compensation mechanism in the semi-insulating material was developed based on these measurements. The free carrier concentration is controlled by the balance between EL2 deep donors and carbon acceptors; furthermore, the incorporation of EL2 is controlled by the melt stoichiometry, increasing as the As atom fraction in the melt increases. As a result, semi-insulating material can be grown only from melts above a critical As composition. The practical significance of these results is discussed in terms of achieving high yield and reproducibility in the crystal growth process.

I. INTRODUCTION

A MAJOR impediment to the development of GaAs integrated circuits and microwave devices has been the lack of a reliable supply of semi-insulating substrates with reproducible and thermally stable [1] properties suitable

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for device fabrication. The liquid encapsulated Czochralski (LEC) technique is currently receiving considerable attention for the production of GaAs crystals because semi-insulating material can be grown without intentional [2] doping, and the technique offers the potential for producing round, large-area substrates with uniform properties at a reasonable cost [3], [4].

The main question surrounding semi-insulating LEC GaAs has concerned the compensation mechanism by which the undoped material is semi-insulating. The understanding of the compensation mechanism has two important practical consequences. First, knowledge of the cause-effect relationships between crystal growth and electrical characteristics of the material would greatly improve the yield of semi-insulating crystals in the growth process, as well as the crystal-to-crystal and wafer-to-wafer reproducibility. Second, this understanding would improve device performance. For example, backgating effects could possibly be diminished by adjusting [5] trap levels in material intended for integrated circuit processing.

It has been shown that the melt stoichiometry [6] is the key parameter which must be controlled to grow undoped semi-insulating LEC GaAs. This finding has led to the development of quantitative model for the compensation mechanism. The purpose of this paper is to give a detailed account of these experimental results and interpretations. In the first section of the paper it is shown that the